REMARKS

N.B. APPLICANT RESPECTFULLY REQUESTS THE EXAMINER, IN THE EXAMINER'S NEXT COMMUNICATION, TO RETURN TO THE UNDERSIGNED ATTORNEY AN INITIALED OF COPY OF THE FORM PTO/SB/08A AND B (MODIFIED) WHICH IS PART OF THE INFORMATION DISCLOSURE STATEMENT FILED ON APRIL 10, 2003. A DUPLICATE COPY OF THE FORM IS ATTACHED FOR THE EXAMINER'S CONVENIENCE.

Claims 1-27 are all the claims pending in the application.

Drawings

Drawing sheet 1/10 has been corrected as requested by the Examiner to add the legend "Prior Art" to Fig. 10.

Claim amendments

Independent claim 1 has been slightly amended to replace the sentence of lines 7 and 8 starting with "interrupting..." by a more appropriate sentence stating : "integrating a first sensed output signal of a first pixel until the end of a first time period and storing the resulting first integrated signal". Similarly, the term "interrupted" in claim 4, line 20, has been replaced by "stored".

Claims 2, 3 and 5 to 27 remain unchanged.

Comments

The notion of "interruption" in claims 1 and 4 has been removed since it appeared to be inappropriate for adequately defining the invention. Indeed, the specification and drawings of the instant application make it clear that the so-called "first integrated signal" is stored at the end of the first time period (t_1-t_0) while the first sensed output signal is still being integrated over time. Integration of the first sensed output signal is thus not *interrupted* at the end of the first time period, but integration continues even after the first integrated signal is

stored. This is particularly clear from the diagrams of Fig. 8 where one clearly sees that integration continues beyond the end of the first time period (i.e., after instant t1 in Fig. 8).

In practice, the so-called integration period is basically the same for all pixels. According to the invention, circuitry is associated with each pixel so as to provide two integrated signal values taken at two distinct instants during integration, namely at the end of the first time period and at the end of the second time period.

This very same idea is expressed in a somewhat different manner in independent claim 10 which has been **allowed** by the Examiner. In claim 10, the sensing device comprises (cf. page 19, lines 29 to 35) :

- *means for resetting said integrating circuits during a resetting period and for releasing these integrating circuits during an integration period;*

- *means for disconnecting a first comparator input of said first comparator circuit from the corresponding integrating circuit at the end of a first time period;*

- *means for storing the resulting integrated signal on the disconnected first comparator input of said first comparator circuit; and*

- *means for latching said first comparator circuit at the end of said integration period.*

Applicant feels that the word, "interruption", formerly present in claims 1 and 4 was misleading and was probably the reason why the Examiner rejected independent parent claim 1. The wording of amended claim 1 now more closely reflects the wording of allowable claim 10.

Claim rejections under 35 U.S.C. § 102

Claims 1-3 and 8 were rejected under 35 USC 102(e) as being anticipated by Stettner et al. (US Pat. 6,362,482). Claims 4 to 7 and 9 are merely objected as being dependent upon a rejected base claim. Claims 10 to 27 are **allowed**. Applicant requests the Examiner to hold in abeyance the rewriting of in claims 4-7 and 9 until the Examiner has had an opportunity to reconsider (and withdraw) the rejection of claims 1-3 and 8.

Stettner et al. discloses a device for high-speed analysis of photon- or particle-generated image data. This device uses a sensor (7) that collects the photons or particles on an array of solid state detectors as electrical analog signals. Readout circuits (17, Fig. 4 or 5) are provided with means for integrating the photon or particle flux signals for a given time frame. The integrated signals are then transferred to an image processing circuit (12, Fig. 7), either directly or via a correction circuit (9, Fig. 6).

According to Stettner et al., integration of the detected signals occurs over a specific time frame (cf. column 8, lines 57-59). At the end of the integration period, the resulting integrated signals are transferred to the following circuits in the chain (correction processor 9 and image processor 12). Integrated signals from at least two pixels are then compared in the image processor (12) in order to perform, for example, edge detection between contiguous pixels (cf. column 9, lines 40 to 53).

It again is stressed that the purpose of the present invention is to perform a comparison of light intensity between pixels, which comparison includes comparing the light intensity value of a first pixel with a **scaled** light intensity value of a second pixel (i.e. the light intensity value of a the pixel multiplied by a so-called scaling factor). As described on page 2, line 36, to page 5, line 35, of the specification of the instant application, such comparison was previously performed, according to US Pat. No. 5,288,993 and 5,703,356,

using specific circuits for performing the scaling operation. There is **no** indication or suggestion in the Stettner et al. reference that a comparison procedure implementing such a scaling operation is performed.

According to the present invention, as in particular defined in claim 1, the comparison procedure with scaling operation is performed by adopting a **time-based scaling scheme** (cf. summary on page 7, lines 17 to 23). This scheme basically consists of comparing the integrated signal values of two pixels taken at two distinct instants during integration of the output signals of the two pixels, i.e., at the end of first and second distinct time periods. The scaling factor is thus determined by the ratio between the second and first time periods (cf. expression (9) on page 14 of the specification of the instant application).

The Stettner et al. reference merely discloses a procedure according to which detected signals are integrated over time during a specific time frame (i.e., the integration time is the same for all pixels) and, thereafter, transferred to another processing circuit where comparison of the integrated signals of contiguous pixels is performed. There is clearly **no** indication or suggestion that comparison is performed between a first integrated signal of a first pixel stored at the end of a first time period and a second integrated signal of a second pixel obtained following continuation of the integration until the end of a second time period.

The **absence** of any time-based scaling scheme in the Stettner et al. reference is evidenced by the fact that all readout unit cells (17, cf. Fig 4 or 5) in the readout circuit (7) are identical and each provide only a single integrated signal value to the subsequent stages, namely the integrated signal value at the end of the integration period. There is clearly **no** indication or suggestion that one readout unit cell does or could provide an integrated signal value taken at the end of a time period which is different from the time period of another

readout unit cell, as the Examiner seems to suggest. On the **contrary**, everything in this reference at least implies that the time periods are the same for all readout unit cells.

It is, moreover, clear that the solution proposed in the Stettner et al. reference does **not** implement any scaling scheme at all. It is for instance clearly stated on column 14, lines 41 to 64, that the signals from the surrounding pixels (Vdtop, Vdbom, Vdrig, Vdlef) are compared against the signal (Vcen) of the center reference pixel and that an output is generated if any of the signals of the surrounding pixels are less than the center reference pixel voltage (cf. in particular column 14, lines 43 to 52). There is clearly **no** indication or suggestion of any sort of scaling factor applied to any of the signals prior to comparison.

Thus, Applicant respectfully submits that claims 1-3 and 8 are not anticipated by (and would not have been obvious over) the disclosure of Stettner et al. That is, this reference does not disclose, either expressly or inherently, or suggest each limitation of each of the claims 1-3 and 8, or in other words, each of these claims is not readable, either expressly or inherently, on (and would not have been obvious over) the disclosure of Stettner et al.

Therefore, Applicant respectfully requests the Examiner to reconsider and withdraw the rejection under 35 U.S.C. § 102(e), and to find the application to be in condition for allowance with all of claims 1-27.

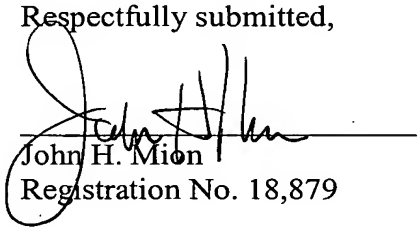
If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to **call the undersigned attorney** to discuss any unresolved issues and to expedite the disposition of the application.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the

Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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